FACULTY OF ENGINEERING

Scheme of Instruction & Examination

(AICTE Model Curriculum for the Academic Year 2019-2020)

and

Syllabus

M.E. I to IV Semester

of

Two Year Post Graduate Degree Programme

in

Electronics and Communication Engineering
Specialization in Embedded Systems and VLSI Design

(With effect from the academic year 2019– 2020)
(As approved in the faculty meeting held on 25-06-2019)

Issued by

Dean, Faculty of Engineering

Osmania University, Hyderabad – 500 007

2019

SCHEME OF INSTRUCTION & EXAMINATION
M.E. (Electronics and Communication Engineering) I – Semester
Specialization in Embedded Systems and VLSI Design

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
Theory Courses										
1	Core	Program Core – I	3	1	-	4	30	70	3	4
2	Core	Program Core – II	3	-	-	3	30	70	3	3
3	Elective	Professional Elective – I	3	-	-	3	30	70	3	3
4	Elective	Professional Elective – II	3	-	-	3	30	70	3	3
5	MC or OE	Mandatory Course / Open Elective*	3	-	-	3	30	70	3	3
6	Audit	Audit Course – I	2	-	-	2	30	70	3	0
Practical/ Laboratory Courses										
7	Lab-I	Laboratory – I	-	-	2	2	25	50	3	1
8	PC 3354 EV	Seminar	-	-	2	2	25	50	3	1
		Total	**17**	**01**	**04**	**22**	**230**	**520**		**18**

PC: Program Core **PE:** Professional Elective **OE**: Open Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination (Univ. Exam)

Note:

1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. * If the Mandatory Course is offered in I-Semester, the Open Elective course should be offered in II-semester. If Open Elective course is offered in I-Semester, then the Mandatory Course should be offered in II- semester.
4. ** Open Elective Subject is not offered to the students of ECE Department.

SCHEME OF INSTRUCTION & EXAMINATION
M.E. (Electronics and Communication Engineering) II – Semester
Specialization in Embedded Systems and VLSI Design

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
Theory Courses										
1	Core	Program Core – III	3	1	-	4	30	70	3	4
2	Core	Program Core – IV	3	1	-	4	30	70	3	4
3	Elective	Professional Elective – III	3	-	-	3	30	70	3	3
4	MC or OE	Mandatory Course / Open Elective	3	-	-	3	30	70	3	3
5	Audit	Audit Course – II	2	-	-	2	30	70	3	0
Practical/ Laboratory Courses										
6	Lab-II	Laboratory – II	-	-	2	2	25	50	3	1
7	Lab-III	Laboratory – III	-	-	2	2	25	50	3	1
8	PC 3355 EV	Mini Project with Seminar	-	-	4	4	25	50	3	2
		Total	**14**	**02**	**08**	**24**	**225**	**500**		**18**

PC: Program Core **PE:** Professional Elective **OE**: Open Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination (Univ. Exam)

Note:

1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. ** Open Elective Subject is not offered to the students of ECE Department.

SCHEME OF INSTRUCTION & EXAMINATION
M.E. (Electronics and Communication Engineering) III – Semester
Specialization in Embedded Systems and VLSI Design

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
Theory Courses										
1	Elective	Professional Elective – IV	3	-	-	3	30	70	3	3
2	Elective	Professional Elective – V	3	-	-	3	30	70	3	3
3	PC 3356 EV	Major Project Phase – I	-	-	20	20	100	-	3	10
		Total	**06**	**-**	**20**	**26**	**160**	**140**		**16**

M.E. (Electronics and Communication Engineering) IV – Semester
Specialization in Embedded Systems and VLSI Design

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
Theory Courses										
1	PC 3357 EV	Major Project Phase – II (Dissertation)	-	-	32	32	-	200	3	16
		Total	**-**	**-**	**32**	**32**	**-**	**200**		**16**

PC: Program Core **PE:** Professional Elective **OE**: Open Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination (Univ. Exam)

Note:

1. Each contact hour is a Clock Hour
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. ** Open Elective Subject is not offered to the students of ECE Department.
4. The students who are willing to register for MOOCs in the M.E. (ES & VLSI) III – semester instead of Professional Electives – IV & V, should register for those of the courses, approved by the CBoS, OU and respective college MOOCs Coordinator. Those students are strictly not permitted to appear for either CIE or SEE of Professional Electives – IV & V if they abstain from attending the semester class work. Further, for students willing to appear for both MOOCS and Professional Electives, they should fulfill the minimum attendance criteria.

List of subjects of Professional Core

S. No.	Course Code	Course Title
1	PC 3301 EV	Micro Controllers for Embedded System Design
2	PC 3302 EV	Digital IC Design
3	PC 3303 EV	Real Time Operating System
4	PC 3304 EV	Analog and Mixed Signal IC Design

List of subjects of Professional Electives I to V

S. No.	Course Code	Course Title
1	PE 3316 EV	Field Programmable Gate Arrays
2	PE 3317 EV	VLSI Physical Design
3	PE 3318 EV	Low Power VLSI Design
4	PE 3319 EV	SoC Design
5	PE 3320 EV	Global & Regional Navigational Satellite Systems
6	PE 3321 EV	Optical Fibre Communication Systems
7	PE 3322 EV	Network Security & Cryptography
8	PE 3323 EV	Communication Buses & Interfaces
9	PE 3324 EV	Communication networks
10	PE 3325 EV	Smart Sensors and Internet of Things
11	PE 3116 DS	Advanced Digital Design with Verilog HDL
12	PE 3119 DS	Advanced Computer Organisation
13	PE 3121 DS	Wireless Mobile Communication Systems
14	PC 3102 DS	Digital System design (Elective)
15	PC 3104 DS	Digital Signal Processors (Elective)

List of Mandatory Courses

S. No.	Course Code	Course Title
1	MC 5161 ME	Research Methodology & IPR

List of Open Electives

S. No.	Course Code	Course Title
1	OE 9101 CE	Cost Management of Engineering Projects
2	OE 9102 CS	Business Analytics
3	OE 9103 EC**	Embedded System Design
4	OE 9104 EE	Waste to Energy
5	OE 9105 ME	Industrial Safety

Note: ** Open Elective Subject is not offered to the students of ECE Department.

List of subjects of Audit Course-I

S. No.	Course Code	Course Title
1	AD 9001 HS	English for Research Paper Writing
2	AD 9002 CE	Disaster Management
3	AD 9003 HS	Sanskrit for Technical Knowledge
4	AD 9004 HS	Value Education

List of subjects of Audit Course-II

S. No.	Course Code	Course Title
1	AD 9011 HS	Constitution of India and Fundamental Rights
2	AD 9012 HS	Pedagogy Studies
3	AD 9013 HS	Stress Management by Yoga
4	AD 9014 HS	Personality Development through life Enlightenment Skills

List of Laboratory Courses

S. No.	Lab No.	Course Code	Course Title
1	I	PC 3351 EV	Embedded Systems Lab
3	II	PC 3352 EV	Real Time Operating Systems Lab
4	III	PC 3353 EV	VLSI Lab

Course Code	Course Title						Core/Elective
PC 3301 EV	**Micro Controllers for Embedded System Design**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**1**	**-**	**-**	**30**	**70**	**4**

Course Objectives

- Detailed overview of important concepts of Embedded system
- Analyse PIC microcontroller, its features and programming
- Describe ARM Microcontroller architectural details and instruction set
- Understand ARM Memory management
- Learn the techniques to develop an embedded system and case studies

Course Outcomes

After completing this course, the student will be able to:

1. Define an embedded system with an overview of important concepts and trends in the design process along with the challenges faced in the embedded systems design.
2. Understand the architecture of PIC 18 Microcontroller, its features and programming.
3. Understand ARM Design Philosophy, architectural details, instruction set and ARM Memory Management.
4. Analyse and compare the utility and effectiveness of various debugging tools and techniques.
5. Design a real time based embedded system in the area of communication, automotive, etc.

UNIT I

Introduction to Embedded Systems: Overview of Embedded System Architecture, Challenges & Trends of Embedded Systems, Hardware Architecture, Software Architecture. Application areas of Embedded Systems and Categories of Embedded Systems. Embedded System Design and Co-Design issues and Design Cycle Process

UNIT II

PIC 18: Family Overview, Architecture, Instruction Set, Addressing modes. Timers, interrupts of PIC 18, Capture/Compare and PWM modules of PIC 18

UNIT III

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT IV

ARM Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instruction Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions. Exception and interrupt handling.

ARM Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation Access Permissions, Context Switch.

UNIT V

Embedded Software Development Tools, Host and Target Machines, Linkers/Locators for Embedded Software, Getting Embedded Software into the Target System. Debugging Techniques.

Case Studies: Design of Embedded Systems using Microcontrollers – for applications in the area of communication and automotive. (GSM/GPRS, CAN, ZigBee)

Suggested Reading:

1. Raj Kamal, *Embedded Systems – Architecture, Programming and Design*, 2nd Edition, TMH, 2008.
2. Andrew N. Sloss, Dominic Symes, Chris Wright, *ARM Systems Developer's Guides – Designing & Optimizing System Software*, Elsevier, 2008.
3. Mazidi, MCKinlay and Danny Causey, *PIC Microcontrollers and Embedded Systems*, Pearson Education, 2007
4. David.E. Simon, *An Embedded Software Primer*, 1st Edition, Pearson Education, 1999
5. Jonathan W. Valvano, *Embedded Microcomputer Systems, Real Time Interfacing*, Thomas Learning, 1999.

Course Code	Course Title						Core/Elective
PC 3302 EV	**Digital IC Design**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**1**	**-**	**-**	**30**	**70**	**4**

Course Objectives:

- Study the secondary effects of MOSFETS in DSM regime, perform timing analysis and size the inverters for optimum path delay
- Learn the Combinational Logic Design in CMOS
- Understand the sequential circuit design and the performance parameters.
- Describe the design of arithmetic building blocks
- Study the semiconductor memory design

Course Outcomes

After completing this course, the student will be able to:

1. Appreciate the secondary effects of MOSFETS in DSM regime, perform timing analysis and size the inverters for optimum path delay
2. Perform path optimization of CMOS gates with Logical Effort
3. Compute delay and power dissipation in both dynamic and static CMOS designs, and apply pipelining techniques to optimize Sequential Circuits
4. Design a simple data path for a processor and apply power reduction techniques
5. Design a 6T SRAM cell and organize a memory bank

UNIT – I

Introduction to DSM CMOS Digital IC design: Quality Metrics, Trends, MOSFET secondary effects, Simple Interconnect Wire models, Design rules, Sub-threshold Conduction. CMOS Inverter – Static and Dynamic Behaviour, Performance, Power and Delay characteristics, NMOS and Pseudo-NMOS Inverters, Sizing of Inverters, Tristate Inverters. Switching Time analysis, Detailed Load Capacitance Calculation, Inverter Sizing for Optimal Path Delay.

UNIT – II

Designing Combinational Logic in CMOS: Static CMOS design: Complimentary CMOS, Rationed Logic, Pass Transistor Logic, Transmission Gate Logic, Optimizing Paths with Logical effort.

Dynamic CMOS Design: Basic Principles, Speed and Power dissipation in Dynamic Logic, Signal Integrity Issues, Cascading Dynamic Gates

UNIT – III

Designing Sequential Circuits: Static Latches and registers, Dynamic Latches and registers, Alternative Register styles, Pipelining to optimize Sequential Circuits, Non-bistable sequential Circuits. Coping with Interconnects: Capacitive, Resistive and Inductive parasitic, Advanced Interconnect Techniques, Power Grid and Clock design: Power Distribution Design, Clocking and Timing Issues, Phase-Locked Loops / Delay Locked Loops.

UNIT – IV

Designing Arithmetic Building Blocks: Data paths in Digital Processor Architectures, The Adder, The Multiplier, The Shifter and The Comparator. Power and Speed Trade-offs in Data path Operators: Design-Time Power Reduction Techniques, Run-Time Power Management, Reducing the Power in Standby (or Sleep) Mode. Power Grid and Clock Design: Power Distribution Design, Clocking and Timing Issues

UNIT – V

Semiconductor Memory Design: Introduction: Memory Organization, Types of memory, memory Timing Parameters, MOS Decoders. SRAM Cell Design: Read Write Operations, SRAM Cell Layout

Suggested Reading:

1. Jan M Rabaey, Anantha Chandrakasan and B. Nikolic, "Digital Integrated Circuits – A Design Perspective", Second Edition, PHI/ Pearson, 2003.
2. David A Hodges, Horace G Jackson and Resve A Saleh, "Analysis and Design of Digital Integrated Circuits in DSM Technology", 3rd Edition, Tata McGraw Hill, 2008.
3. Wayne Wolf, *Modern VLSI Design*, 3rd edition, Pearson Education, 1997.
4. Neil H E Weste Kamran Eshraghian, *Principles of CMOS VLSI Design a system perspective*, 3rd edition, Pearson, 2005.
5. K. Eshraghian, A. Pucknell, *Essentials of VLSI Circuits and Systems*, PHI, 2005.

Course Code	Course Title						Core/Elective
PC 3303 EV	**Real Time Operating Systems**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**1**	**-**	**-**	**30**	**70**	**4**

Course Objectives

- Understand concepts of OS and RTOS
- Describe UNIX OS
- Distinguish between Hard and Soft RTOS
- Analyse the concept of Embedded RTOS
- Explore VxWorks

Course Outcomes

After completing this course, the student will be able to:

1. Describe the features of UNIX operating system and differentiate between UNIX and POSIX.
2. Differentiate between Hard and Soft Real time systems and familiarize with classical Uni-processor scheduling algorithms
3. Understand the concepts of Real time operating systems and analyse the Inter process communication.
4. Explain the features of VxWorks and compare the commercially available RTOS's
5. Understand the debugging tools and cross development environment.

UNIT I

Brief Review of Unix Operating Systems (Unix Kernel – File system, Concepts of – Process, Concurrent Execution & Interrupts. Process Management – forks & execution. Programming with system calls, Process Scheduling. Shell programming and filters).

Portable Operating System Interface (POSIX) – IEEE Standard 1003.13 & POSIX real time profile. POSIX versus traditional Unix signals, overheads and timing predictability.

UNIT II

Hard versus Soft Real-time systems – examples, Jobs & Processors, Hard and Soft timing constraints, Hard Real-time systems, Soft Real-time systems. Classical Uniprocessor Scheduling Algorithms – RMS, Preemptive EDF, Allowing for Preemptive and Exclusion Condition.

UNIT III

Concept of Embedded Operating Systems, Differences between Traditional OS and RTOS. Real- time System Concepts, RTOS Kernel & Issues in Multitasking – Task Assignment, Task Priorities, Scheduling, Intertask Communication & Synchronization – Definition of Context Switching, Foreground ISRs and Background Tasks. Critical Section – Reentrant Functions, Interprocess Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.

UNIT IV

VxWorks – POSIX Real Time Extensions, timeout features, Task Creation, Semaphores (Binary, Counting), Mutex, Mailbox, Message Queues, Memory Management – Virtual to Physical Address Mapping.

UNIT V

Debugging Tools and Cross Development Environment – Software Logic Analyzers, ICEs. Comparison of RTOS – VxWorks, µC/OS-II and RT Linux for Embedded Applications.

Suggested Reading:

1. Jane W.S. Liu, Real Time Systems, Pearson Education, Asia, 2001.
2. Betcnhof, D.R., Programming with POSIX threads, Addison - Wesley Longman, 1997.
3. Wind River Systems, VxWorks Programmers Guide, Wind River Systems Inc.1997.
4. Jean.J. Labrosse, MicroC/OS-II, The CMP Books.
5. Real Time Systems, C.M. Krishna and G. Shin, McGraw-Hill Companies Inc., McGraw Hill International Editions, 1997.

Course Code	Course Title						Core/Elective
PC 3304 EV	**Analog and Mixed Signal IC Design**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Learn the concepts of advanced current mirrors and band-gap reference circuits.
- Analyse applications of Op amp: comparator and oscillator
- Familiarize with switched capacitor based circuits.
- Distinguish between the features of mixed signal circuits and other circuits.
- Analyse mixed signal circuits like switched capacitor circuits, data converters etc., starting from fundamentals.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the basic concepts of CMOS circuits, analyse and design current sources/sinks/mirrors
2. Understand the concepts of OPAMPs and its characteristics and Analyse the operation of comparators and various oscillators.
3. Emphasize the concepts of switched capacitor circuits
4. Comprehend the features of sample and hold circuits and apply them to design Nyquist rate data converter circuits.
5. Analyze and design oversampling rate data converter circuits.

UNIT I

Brief Review of Small Signal and Large Signal Model of BJTs and MOSFETs. Current Mirrors and Single Stage Amplifiers – Simple CMOS current mirror, common source amplifier, source follower, common gate amplifier, cascode amplifiers. Source degenerated current mirrors. High out impedance – current mirrors, cascode gain stage Wilson current mirror, MOS differential pair and gain stage. Bipolar current mirrors – bipolar gain stages. Differential pairs with current mirror loads MOS and bipolar widlar current sources,

UNIT II

Operational amplifiers, Basic two stage MOS Operational amplifier–Characteristic parameters, two stage MOS Op-Amp with Cascodes. MOS Telescopic-cascode Op- Amp. MOS Folded cascode op-amp. MOS Active Cascode Op-Amp.Fully differential folded cascode op-amp. Current feedback op-amps. Stability and frequency compensation of op- amps. Phase margin and noise in op-amps.

UNIT – III

Comparators: Op-Amp Based Comparators, Charge Injection Errors – Latched Comparators – CMOS and BiCMOS Comparators – Bipolar Comparators.

Switched capacitor circuits: Basic building blocks; basic operation and analysis, inverting and non-inverting integrators, signal flow diagrams, first order filter.

Sample and hold circuits - Performance requirements, MOS sample and hold basics, clock feed through problems,

UNIT – IV

S/H using transmission gates, high input impedance S/H circuits, improved S/H circuits from the point of slewing time, clock feed through cancellations. Data converter fundamentals - performance characteristics, ideal D/A and A/D converters, quantization noise. Nyquist rate D/A converters – decoder based converter, binary-scaled converters. Thermometer code converters, current mode converters.

UNIT – V

Nyquist rate A/D Converters: Integrated converters – successive approximation converters, cyclic A/D converters, Flash or parallel converters, Two step A/D converters, pipelined A/D converters. Over sampling converters. Over sampling without noise shaping over sampling and with noise shaping, system architecture – digital decimation filters.

Suggested Reading:

1. Paul.R. Gray & Robert G. Major, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004
3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw Hill. 2002
4. Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.
5. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.

Course Code	Course Title						Core/Elective
PE 3316 EV	**Field Programmable Gate Arrays**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Learn Application Specific IC (ASIC) fundamentals
- Describe FPGA
- Calculate power consumption of designed IC
- Understand Interconnection, Placement and Routing schemes.
- Learn Verification and testing schemes.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the design flow of ASICs and identify the implementation tools required for simulation and synthesis of FPGA Design
2. Describe the architecture of FPGA's.
3. Explain the physical design of FPGA's and CAD tools for low level design entry.
4. Estimate the placement & routing algorithms.
5. Validate the digital design and discuss the general design issues.

UNIT I

Introduction to ASIC's: Types of ASIC's, ASIC design flow, Economies of ASIC's, Programmable ASIC's: CPLD and FPGA. Commercially available CPLD's and FPGA's: XILINX, ALTERA, ACTEL. FPGA Design cycle, Implementation tools: Simulation and synthesis, Programming technologies. Applications of FPGAs

UNIT II

FPGA logic cell for XILINX, ALTERA and ACTEL ACT, Technology trends, Programmable I/O blocks, FPGA interconnect: Routing resources, Elmore's constant, RC delay and parasitic capacitance, FPGA design flow, Dedicated Specialised components of FPGAs

UNIT III

FPGA physical design, CAD tools, Power dissipation, FPGA Partitioning, Partitioning methods. Floor planning: Goals and objectives, I/O, Power and clock planning, Low-level design entry.

UNIT IV

Placement: Goals and objectives, Placement algorithms: Min-cut based placement, Iterative Improvement and simulated annealing.

Routing, introduction, Global routing: Goals and objectives, Global routing methods, Back-annotation. Detailed Routing: Goals and objectives, Channel density, Segmented channel routing, Maze routing, Clock and power routing, Circuit extraction and DRC.

UNIT V

Verification and Testing: Verification: Logic simulation, Design validation, Timing verification. Testing concepts: Failures, Mechanism and faults, Fault coverage. Design Applications: General Design issues, Counter Examples, A Fast DMA controller, Designing adders and accumulators with Xilinx Architecture

Suggested reading:

1. Pak and Chan, Samiha Mourad, *Digital Design using Field Programmable Gate Arrays*, Pearson Education, 1st edition, 2009.
2. Michael John Sebastian Smith, *Application Specific Integrated Circuits*, Pearson Education Asia, 3rd edition 2001.
3. S. Trimberger, Edr, *Field Programmable Gate Array Technology*, Kluwer Academic Publications, 1994.
4. John V. Oldfield, Richard C Dore, *Field Programmable Gate Arrays*, Wiley Publications.

Course Code	Course Title						Core/Elective
PE 3317 EV	**VLSI Physical Design**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Use graph theory in physical design
- Learn various optimization methods
- Understand different techniques for placement and routing

Course Outcomes

After completing this course, the student will be able to:

1. Appreciate various Algorithms used for system design
2. Comprehend the basic cell layout design and Placement and routing
3. Understand different levels of modelling and synthesis.

UNIT-I

VLSI Design Automation Tools: Algorithms and System Design- Structural and Logic Design- Transistor Level Design- Layout Design- Verification Methods- Design Management Tools.

UNIT-II

Layout Compaction-Placement and Routing: Design Rules- Symbolic Layout- Application of Compaction- Formulation Methods- Algorithms for Constrained Graph Compaction- Circuit Representation- Wire Length Estimation- Placement Algorithms- Partitioning Algorithms.

UNIT-III

Floor Planning and Routing: Floor Planning concepts- Shape Functions and Floor Planning Sizing- Local Routing- Area Routing- Channel Routing- Global Routing - Global Routing and its Algorithms.

UNIT-IV

Simulation and Logic Synthesis: Gate Level and Switch Level Modelling and Simulation- Introduction to Combinational Logic Synthesis. ROBDD Principles- Implementation- Construction and Manipulation, Two Level Logic Synthesis.

UNIT-V

High-Level Synthesis: Hardware Model for High Level Synthesis- Internal Representation of Input Algorithms Allocation- Assignment and Scheduling, Scheduling Algorithms- Aspects of Assignment. High Level Transformation.

Suggested Reading:

1. S.H. Gerez “Algorithms for VLSI Design Automation
2. K.K Parhi “VLSI Digital Signal processing”. (1999), John-Wiley
3. N.A. Sherwani “Algorithms for VLSI Physical Design Automation”, John Wiley, 1998
4. S.M Sait and H. Youssef “VLSI Physical Design Automation”, World Science, 1999
5. M. Sarrafzadeh “Introduction to VLSI Physical Design”, McGraw Hill (IE),1996

Course Code	Course Title						Core/Elective
PE 3318 EV	**Low Power VLSI Design**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- Characterize and model power consumption & understand the basic analysis methods.
- Understand leakage sources and reduction techniques.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the need for low power design and different strategies for low power.
2. Estimate the Power at various levels of abstraction.
3. Optimize the power at various levels of the design using power optimization techniques.
4. Describe the energy recovery circuit design
5. Estimate the software design for low power.

UNIT - I

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

UNIT - II

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

UNIT - III

Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. Tolerable skew, chip & package co-design of clock network.

UNIT - IV

Logic Synthesis for Low Power: Power Estimation Techniques, Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

UNIT -V

Low Power Memory Design: Sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM, low power DRAM circuits, low power SRAM circuits.

Suggested Reading:

1. P. Rashinkar, Paterson and L. Singh, "*Low Power Design Methodologies*", Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, "*Low power CMOS VLSI circuit design*", John Wiley sons Inc.,2000.
3. J.B.Kulo and J.H Lou, *"Low voltage CMOS VLSI Circuits*", Wiley, 1999.
4. A.P. Chandrasekaran and R.W. Broadersen, "*Low power digital CMOS design*", Kluwer,1995
5. Gary Yeap, "*Practical low power digital VLSI design*", Kluwer, 1998.

Course Code	Course Title						Core/Elective
PE 3319 EV	**SoC Design**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Understand Integration of hardware and software on a single chip
- Describe various processors
- Design of Memory for SoC
- Familiarize with Interconnection of various devices and reconfiguration
- Explore various application of system on single chip

Course Outcomes

After completing this course, the student will be able to:

1. Apply fundamental knowledge of digital logic design to modelling and analysis of low power in processor design.
2. Understand the design concepts of processor, pipelining concepts, ARM Development Tools and Interfacing ARM with Co-processors.
3. Understand the concepts of Memory Hierarchy, Cache design and Memory Management.
4. Develop an understanding of various interconnect schemes for system Development.
5. Design a simple SoC for reconfigurability/low power/ASIP/NISC etc.

UNIT I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures,
Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT IV

Interconnect Customization and Configuration: Inter Connect Architectures,

Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Suggestive Reading:

1. Ricardo Reis, "*Design of System on a Chip: Devices and Components*, 1st Ed., Springer, 2004.
2. Michael J. Flynn and Wayne Luk, *Computer System Design System-on-Chip*, Wiley India Pvt. Ltd.
3. Steve Furber, *ARM System on Chip Architecture*, 2nd Ed., Addison Wesley Professional, 2000.
4. Jason Andrews, *Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)*, Newnes, BK and CDROM.
5. Prakash Rashinkar, Peter Paerson and Leena Singh L, *System on Chip Verification – Methodologies and Techniques*, Kluwer Academic Publishers, 2001.

Course Code	Course Title						Core/Elective
PE 3320 EV	**Global and Regional Navigation Satellite Systems**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Familiarize with GNNS fundamentals
- Learn GNSS signal structure, errors and their modelling
- Understand GPS errors and their modelling techniques
- Study GPS integration and data processing techniques
- Analyse GNSS augmentation and Regional navigation systems

Course Outcomes

After completing this course, the student will be able to:

1. Understand the principle & operation of GPS.
2. Frame various co-ordinate systems for estimating positions.
3. Estimate the various errors and their effect on position estimation.
4. Use GPS in various fields such as navigation GIS etc.
5. Apply DGPS principle and can also analyze various augmentation system.

UNIT I

GPS fundamentals: GPS principle of operation, architecture, operating frequencies, orbits, Keplerian elements. Solar and Sidereal day, GPS and UTC Time

Other GNNSs: Architecture and features of Russian Global Navigation Satellite System (GLONASS), European Navigation System (Galileo), Chinese Global Navigation System (BeiDou-2/COMPASS).

UNIT II

GNSS Signals: Original and modernized GPS, GLONASS and Galileo signal structure, Signal components and modulation schemes. Important components of a receiver for the acquisition and tracking of GPS signals.

GNSS Datums: Datums used for GPS and Galileo (ECEF and WGS 84). Datum used by Russian GLONASS and Indian Datums.

UNIT III

GPS Error Models: Ionospheric error, Tropospheric error, Ephemeris error, Clock errors, Satellite and receiver instrumental biases, Antenna Phase center variation, multipath; estimation of Total Electron Content (TEC) using dual frequency measurements, Various DOPs, UERE. Spoofing and Anti-spoofing. Link budget. Klobuchar model, Hopfield model and modelling of multipath error.

UNIT IV

GPS data processing: RINEX Navigation and Observation formats, Code and carrier phase observables, linear combination and derived observables, Ambiguity resolution, cycle slips, Position estimation.

GPS integration: GPS/GIS, GPS/INS, GPS/pseudolite, GPS/cellular.

UNIT V

Augmentation systems: Relative advantages of SBAS and GBAS, Wide area augmentation system (WAAS) architecture, GAGAN, EGNOS and MSAS. Principle of operation of DGPS, architecture and errors. Local area augmentation system (LAAS) concept.

Regional Navigation Satellite Systems (RNSS): Chinese Area Positioning System (CAPS). Indian Regional Navigation Satellite System (IRNSS), Japan's Quasi-Zenith Satellite System (QZSS).

Suggested Reading:

1. Pratap Misra and Per Enge, *Global Positioning System Signals, Measurements, and Performance*, Ganga-Jamuna Press, Massachusetts, 2001.
2. Rao G.S., *Global Navigation Satellite Systems - With Essentials of Satellite Communications*, Tata McGraw Hill, 2010.
3. B. Hofmann Wollenhof, H. Lichtenegger, and J. Collins, *GPS Theory and Practice*, Springer Wien, New York, 2000.
4. Ahmed El-Rabbany, *Introduction to GPS*, Artech House, Boston, 2002.
5. Bradford W. Parkinson and James J. Spilker, *Global Positioning System: Theory and Applications*, Volume I and II, American Institute of Aeronautics and Astronautics, Inc., Washington, 1996.

Course Code	Course Title						Core/Elective
PE 3321 EV	**Optical Fibre Communication Systems**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Analyse optical fibre as wave guide
- Learn various optical sources and detectors used in optical signal transmission
- Familiarize with various components used in optical communication like, preamplifiers, links
- Estimate Performance evaluation of optical communication
- Explore applications of optical communication in Local Area Networks

Course Outcomes

After completing this course, the student will be able to:

1. Comprehend the key concepts of modes and linearly polarized modes. Distinguish ray propagation in single mode and graded index fibers.
2. Describe the effects of dispersion in optical fibers due to materials, waveguide, polarization modes
3. Choose direct and indirect band gap materials, light source materials. Understand structures of LED, Laser diodes and the concepts of quantum laser, temperature effects and amplifiers.
4. Describe the working of PIN, APD diodes and estimate noise performance of photo detector response time. Categorize different error sources and comprehend the concept of probability of error and quantum limit
5. Analyze point to point link to estimate power link budget and rise time budget. Understand the operational details of Erbium doped fiber amplifiers and basics of SONET/SDH network.

UNIT I

Optical Fibres: Fibre Structures, Wave-guiding and fabrications, Overview of Optical fibre communications, Elements of an Optical fibre transmission Link, Nature of light, Basic optical laws and definitions, Modes and configurations, Mode theory of circular wave guides, Single, Multi mode step index and Graded Index Fibres, Fibre materials. Signal degradation in Optical Fibres. Dispersion, Pulse broadening in graded index fibres, Mode coupling, Design optimization of single mode Fibres.

UNIT II

Optical Sources & Detectors: Semiconductors as optical Sources and their fabrication. LED and Laser diodes, Linearity of sources, Modal, Partition and reflection noise, Physical principles of PIN and APD, Photo detector noise, detector response time, Avalanche multiplication noise, Temperature effect on avalanche gain, Comparison of Photo detectors.

UNIT III

Optical Fibre communication: Basic communication system, Fundamental receiver operation, Digital receiver performance calculations. Preamplifiers types, Analog receivers. Fibre Links: Point to point links, Line coding, Error correction, Noise effects on digital transmission system performance. Overview of analog links, Carrier noise ratio in analog systems.

UNIT IV

Multi-channel transmission techniques: WDM concepts and components. Operational principles of WDM, Passive components, Tunable sources, Tunable filters, Introduction of optical amplifiers.

UNIT V

Optical Networks: Basic Networks, SONET/SDH, Broadcast and select WDM networks, Wavelength Routed Networks, Nonlinear effects on Network Performance, Performance of EDFA+WDM systems, Optical CDMA, Ultrahigh capacity Networks.

Suggested Reading:

1. Djafar K. Mynbaev Lowell I. Scheiner "Fibre Optic Communications Technology", Pearson Education Asia.
2. Senior John M. "Optical Fibre Communications Principles and Practice", Prentice Hall India, second edition, 1996
3. Keiser Gerd, "Optical Fibre Communications", McGraw Hill, second edition,1991
4. William S and Ivan D, "OFDM for Optical Communications", Academic Press: Elsevier, 2010.
5. Ivan P K, Tingye L, and Alan E W, "Optical Fiber Communications VIB: Systems and Networks", 6th Edition, Academic Press: Elsevier, 2013.

Course Code	Course Title						Core/Elective
PE 3322 EV	**Network Security and Cryptography**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Identify and utilize different forms of cryptography techniques.
- Incorporate authentication and security in the network applications.
- Distinguish among different types of threats to the system and handle the same.

Course Outcomes

After completing this course, the student will be able to:

1. Compare various cryptography techniques
2. Familiarize with the algorithms used in cryptography
3. Summarize various layers of security

UNIT-I

Security: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT-II

Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT-III

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT-IV

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT-V

Authentication: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

Suggested Reading:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
3. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
4. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
5. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

Course Code	Course Title						Core/Elective
PE 3323 EV	**Communication Buses and Interfaces**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Select a particular serial bus suitable for a particular application.
- Develop APIs for configuration, reading and writing data onto serial bus.
- Design and develop peripherals that can be interfaced to desired serial bus.

Course Outcomes

After completing this course, the student will be able to:

1. Familiarize with various serial and parallel buses
2. Compare serial, parallel and internet enabled system-network protocols.
3. Understand the data streaming serial communication protocols

UNIT-I

Serial Busses: Physical interface, Data and Control signals, features, limitations and applications of RS232, RS485, I^2C, SPI

UNIT-II

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT-III

PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT-IV

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT-V

Data Streaming Serial Communication Protocol: Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

Suggested Reading:

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition
2. Jan Axelson, "USB Complete", Penram Publications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 – 200x
6. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

Course Code	Course Title						Core/Elective
PE 3324 EV	**Communication Networks**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Analyse protocols and algorithms, acknowledge tradeoffs and rationale
- Use routing, transport protocols for the given networking scenario and application
- Evaluate and develop small network applications

Course Outcomes

After completing this course, the student will be able to:

1. Assess the importance of transport services and various elements of transport layer like Connection management, TCP and UDP protocols.
2. Relate the Network Security with Cryptography Symmetric Key and Public Key algorithms, and will appreciate the concept of Digital Signatures and Authentication Protocols.
3. Understand and comprehend the importance of Application layer and Domain Name System, SNMP, E-mail, World Wide Web.

UNIT-I

Introduction to communication networks: Evolution of Network Architecture and services, Performance, Future Network Architectures, key factors Connecting nodes: Connecting links, Encoding, framing, Reliable transmission.

UNIT-II

Overview: Ethernet and Multiple access networks, Wireless networks Queuing models: For a) one or more servers b) with infinite and finite queue size c) Infinite population

UNIT-III

Internetworking: Switching and bridging, IPv4, Addressing, Routing Protocols, Scale issues, Routers - Architecture, IPv6.

End-to-End Protocols: Services, Multiplexing, De-multiplexing, UDP, TCP, RPC, RTP.

UNIT-IV

congestion control and Resource Allocation: Issues, Queuing disciplines, TCP congestion control, Congestion Avoidance

QOS Applications: Domain Name Resolution, File Transfer, Electronic Mail, WWW.

UNIT-V

Multimedia Applications, Network monitoring – Packet sniffing tools such as Wireshark Simulations using NS2/OPNET.

Suggested Reading:

1. Larry L. Peterson, Bruce S, Devie, "Computer Networks", MK, 5th Edition
2. Vijay Ahuja, "Communications Network Design and Analysis of Computer Communication Networks", MGH, International Editions
3. Indra Widjaja "Communication networks", TMH, 2nd Edition
4. Aaron Kershenbaum, "Telecommunication Network Design Algorithms", MGH, International Edition 1993.
5. Douglas E. Comer, "Internetworking with TCP/IP", Pearson Education, 6th Edition
6. Nadar F. Mir, "Computer and Communication Networks", Pearson Education,2007.

Course Code	Course Title						Core/Elective
PE 3325 EV	**Smart Sensors and Internet of Things**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Able to understand the application areas of IoT
- Able to realize the revolution of Internet in Mobile Devices, Cloud & Sensor Networks
- Able to understand building blocks of Internet of Things and characteristics

Course Outcomes

After completing this course, the student will be able to:

1. Understand the working principle of different sensors
2. Familiarise with the characteristics, Modelling and Adoption of smart sensors
3. Determine the features and fabrication techniques of smart sensors

UNIT-I

Environmental Parameters Measurement and Monitoring: Why measurement and monitoring are important, effects of adverse parameters for the living being for IOT

UNIT-II

Sensors: Working Principles: Different types; Selection of Sensors for Practical Applications, Introduction of Different Types of Sensors such as Capacitive, Resistive, Surface Acoustic Wave for Temperature, Pressure, Humidity, Toxic Gas etc.

UNIT-III

Important Characteristics of Sensors: Determination of the Characteristics Fractional order element: Constant Phase Impedance for sensing applications such as humidity, water quality, milk quality Impedance Spectroscopy: Equivalent circuit of Sensors and Modelling of Sensors Importance and Adoption of Smart Sensors

UNIT-IV

Architecture of Smart Sensors: Important components, their features Fabrication of Sensor and Smart Sensor: Electrode fabrication: Screen printing, Photolithography, Electroplating Sensing film deposition: Physical and chemical Vapour, Anodization, Sol-gel

UNIT-V

Interface Electronic Circuit for Smart Sensors and Challenges for Interfacing the Smart Sensor, Usefulness of Silicon Technology in Smart Sensor and Future scope of research in smart sensor

***Suggested Reading*:**

1. Yasuura, H., Kyung, C.-M., Liu, Y., Lin, Y.-L., Smart Sensors at the IoT Frontier, Springer International Publishing
2. Kyung, C.-M., Yasuura, H., Liu, Y., Lin, Y.-L., Smart Sensors and Systems, Springer International Publishing

Course Code	Course Title						Core/Elective
PE 3116 DS	**Advanced Digital Design with Verilog HDL**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Describe modelling styles of Verilog HDL
- Design modelling of Combinational and Sequential Logic modules
- Learn synthesis and synthesizers
- Understand verification methods and timing analysis
- Demonstrate case studies using Verilog HDL

Course Outcomes

After completing this course, the student will be able to:

1. Describe different modelling styles in Verilog HDL
2. Design Verilog codes of Combinational and Sequential Logic modules
3. Understand the design flow of ASICs and FPGA
4. Learn concept of functional verification and timing analysis
5. Design arithmetic and signal processing modules.

UNIT I

Review of Verilog HDL, Modelling styles: Behavioural, Dataflow, and Structural Modelling, gate delays, switch-level Modelling, Hierarchal structural modelling.

UNIT II

Modelling of basic MSI Combinational Logic modules and Sequential Logic modules. Finite State Machine modelling.

UNIT III

Synthesis: Design flow of ASICs and FPGA based system, design environment and constraints logic synthesizers, Language structure synthesis, coding guidelines for clocks and reset.

UNIT IV

Verification: Functional verification, simulation types, Test Bench design, Dynamic timing analysis, static timing analysis, value change dump (VCD) files. FPGA based design flow- a case study.

UNIT V

Design Examples: Adders and Subtractors, Multiplication and Division Algorithms, ALU, Digital Signal Processing modules: FIR and IIR Filters, Bus structures, Synchronous & Asynchronous data transfer, UART, baud rate generator. A simple CPU design

Suggested Reading:

1. Ming-Bo Lin., *Digital System Designs and Practices Using Verilog HDL and FPGAs*. Wiley, 2008.
2. Michael D. Ciletti, *Advanced Digital Design with the Verilog HDL*", PHI, 2005.
3. Samir Palnitkar, "*Verilog HDL: A Guide to Digital Design and Synthesis*", Pearson Education, 2005.
4. Bhasker J., *Verilog HDL Primer Hardcover*, 2nd Edition, Star Galaxy Publishing ,1999

Course Code	Course Title						Core/Elective
PE 3119 DS	**Advanced Computer Organization**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Identify limitations of different architectures of computer
- Analysis quantitatively the performance parameters for different architectures
- Investigate issues related to compilers and instruction set based on type of architectures.

Course Outcomes

After completing this course, the student will be able to:

1. Comprehend the organization of the CPU and data path design.
2. Understand the concepts of Hardwired and Micro programmed Control Unit design of general purpose computer
3. Describe the memory organization and hierarchy.
4. Discuss I/O Interfacing concepts.
5. Describe the challenges & Limitations of Instruction Level Parallelism

UNIT-I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, operations in the instruction set.

UNIT-II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT-III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT-IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT-V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

***Suggested Reading*:**

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, An Imprint of Elsevier.
2. John P. Shen and Miikko H. Lipasti, "Modern Processor Design : Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw Hill
3. Kai Hwang, Faye A.Brigs., "Computer Architecture, and Parallel Processing", McGraw Hill.,
4. Dezso Sima, Terence Fountain, Peter Kacsuk , "Advanced Computer Architecture – A Design Space Approach", Pearson Education.

Course Code	Course Title						Core/Elective
PE 3121 DS	**Wireless Mobile Communication Systems**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Understand Evolution of Cellular Networks, and review of Cellular concepts
- Learn Large scale Outdoor and Indoor propagation models
- Familiarize with Small scale fading, multipath and Multiple Access techniques
- Learn Modulation techniques for mobile radio.
- Understand Wireless Networking, Systems and Standards

Course Outcomes

After completing this course, the student will be able to:

1. Understand the method of selection and reuse of a set of frequency channels, Base station requirement , signals required for communication and hand over between Base stations.
2. Appreciate and understand the methods of electromagnetic wave propagation in cellular communication. The evaluation of the electromagnetic energy reaching the mobile unit.
3. Identify factors influencing small scale fading, parameters of mobile multipath channel and also understand different multiple access techniques.
4. Understand different spread spectrum like DSSS, FHSS.
5. Understand traffic routing in wireless network, wireless data services and learn about wireless systems and standards like AMPS ,PTACS,GSM and AIN.

UNIT I

Modern Wireless Communication Systems: 1G, 2G, 2.5G, 3G, and 4G technologies.

Cellular Concept: Frequency reuse, Channel assignment strategies, Handoff strategies. Interference and system capacity. Trunking and Grade of service, Improving coverage and capacity in cellular systems

UNIT II

Mobile radio propagation : Large scale propagation free space propagation model. Outdoor propagation models: longely Rice model, Durkin's model, A case study, okumura model, Hata model, PCS Extension to Hata model. Indoor propagation models: partition losses(same floor), partition losses(between floors), log distance path loss model, ericsson multiple breakpoint model, attenuation factor model, signal penetration into buildings.

UNIT III

Small scale fading & multipaths: Factors influencing small scale fading, small scale multipath measurements, parameters of mobile multipath channel. Types of small scale fading.

Multiple Access techniques: FDMA, TDMA, CDMA.

UNIT IV

Modulation techniques for mobile radio: Constant envelop modulation.

Spread Spectrum Modulation Techniques: PN Sequences. Direct Sequence Spread Spectrum (DS-SS), Frequency hopped Spread Spectrum (FH-SS). Performance of Direct Sequence Spread Spectrum. Performance of Frequency hopped Spread Spectrum.

UNIT V

Wireless Networking: Traffic Routing in Wireless Networks, Wireless Data Services. Common Channel Signaling (CCS), ISDN, Broadband ISDN and ATM. Signalling System No 7. SS7 User Part. Services and Performance.

Wireless Systems and Standards: AMPS and ETACS, GSM. Advanced intelligent network (AIN)

Suggested Reading:

1. Rappaport, "*Wireless Communication*", Pearson Education, 2nd edition, 2002.
2. William C. Y. Lee, "*Mobile Cellular Telecommunications: Analog and Digital Systems*", 2nd edition, McGraw-Hill Electronic Engineering Series, 1995.
3. William C.Y. Lee, "*Mobile Communication Engineering*", McGraw Hill, 1997.
4. Mike Gallegher, Randy Snyder, "*Mobile Telecommunications Networking with IS-41*", McGraw Hill 1997.
5. Kernilo, Feher, "*Wireless Digital Communications*", PHI, 2002.

Course Code	Course Title						Core/Elective
PC 3102 DS	**Digital System Design**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Design minimized sequential machines
- Analyse synchronous sequential machines.
- Analyse asynchronous sequential machines.
- Model logical faults for combinational circuits using conventional test generation methods
- Learn basic fault diagnosis algorithms in sequential circuits

Course Outcomes

After completing this course, the student will be able to:

1. Design combinational logic using PLDs
2. Design synchronous and asynchronous sequential circuits
3. Realize algorithmic state machine (ASM) charts of digital circuits
4. Understand concept of fault modelling and test generation techniques.
5. Learn concepts of fault diagnosis in sequential circuits.

UNIT I

Digital Design: Top-Down Modular Combination Logic Design, Combinational circuit Design with Programmable logic Devices (PLDs).

Sequential circuits design: state table, state diagrams. Latches and Flip-Flops- excitation table, characteristic equations - Mealy, Moore models and Sequence detector

Minimization and Transformation of Sequential Machines: The Finite State Model- capabilities and limitations of FSM, state equivalence and machine minimization, Moore and Melay models.

UNIT-II

Analysis and synthesis of synchronous sequential circuits, one hot FSM design method. Finite state controllers Algorithmic State Machine Diagram. Redundant state reduction in completely and incompletely specified circuits, optimal state assignment methods

UNIT-III

Analysis and synthesis of asynchronous sequential circuits: Analysis of pulse mode and fundamental mode circuits. Flow table, state reduction, minimal closed covers, races, cycles and Hazards. Synchronization failure and meta stability.

UNIT-IV

Fault Modelling & Test Pattern Generation: Logic Fault model in combinational circuits – Fault detection and Redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method, and D algorithm. Test generation - Random testing, Transition count testing and Signature analysis.

UNIT-V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of Fault detection experiment.

Suggested Reading:

1. John F. Wakerly, *Digital Design, Principle and Practices*, 3rd Edition, Pearson Education, 2003.
2. CD Victor, P. Nelson, H Troy Nagle, Bill D. Carrol and J David Irwin. *Digital Logic Circuit Analysis and Design*, PHI, 1996.
3. Charles H. Roth, *Fundamentals of Logic Design*, 5th edition, Cengage Learning 2010.
4. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, *Digital Systems Testing and Testable Design*, John Wiley & Sons Inc 1990.
5. Parag.K.Lala, *Fault Tolerant and Fault Testable Hardware Design*, BS Publications, 2007.
6. Biswas N.N. *Logic Design Theory*, PHI, 2001.
7. Zvi Kohavi, S*witching and Finite Automata Theory*, TMH, 2001.

Course Code	Course Title						Core/Elective
PC 3104 DS	**Digital Signal Processors**						**Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Analyse and synthesize signals
- Compute errors caused by conversion
- Describe functional blocks of DSP processor and their use
- Understand processors with examples
- Design various interfacing devices with processor

Course Outcomes

After completing this course, the student will be able to:

1. Determine DFT using direct and FFT methods. Analyse Circular and Linear convolution, and apply for linear filtering.
2. Compute the errors in DSP System Design & Suggest to Design the Accurate DSP Systems.
3. Discuss the Architectural features of programmable DSP devices & Implement various functional units of DSP Systems.
4. Compare & Comprehend the features of Texas based fixed-point & floating-point DSP Processors.
5. Understand various interfacing signals & interface memory and parallel I/O Peripherals to Programmable DSP Devices.

UNIT I

Introduction to Digital Signal Processing: A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT II

Computational Accuracy in DSP Implementation: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing. Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT IV

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices: : Fixed point DSPs – Architecture of TMS 320C5X, C54X Processors , addressing modes, Memory space, Assembly instructions, Program Control ,Pipelining and on-chip peripherals. Floating point DSPs: Architecture of TMS 320 – IX.

UNIT V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices : Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

Suggested Reading:

1. K. Shin, *DSP Applications with TMS 320 Family*, Prentice Hall, 1987.
2. B. Ventakaramani, M. Bhaskar, *Digital Signal Processes, Architecture Processing and Applications*, Tata McGraw Hill, 2002.
3. Lapsley et al., *DSP Processor Fundamentals, Architectures & Features*, S. Chand & Co, 2000.
4. Avtar Singh and S. Srinivasan, *Digital Signal Processing*, Thomson Publications, 2004.
5. Woon-Seng Gan, Sen M. Kuo, *Embedded Signal Processing with the Micro Signal Architecture*, Wiley-IEEE Press, 2007.

Course Code	Course Title						Core/Elective
MC 5161 ME	**Research Methodology and IPR**						**Mandatory Course**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

To make students to

- Motivate to choose research as career
- Formulate the research problem, prepare the research design
- Identify various sources for literature review and data collection report writing
- Equip with good methods to analyse the collected data
- Know about IPR copyrights

Course Outcomes

At the end of this course, students will be able to**:**

1. Define research problem, review and asses the quality of literature from various sources
2. Improve the style and format of writing a report for technical paper/ Journal report, understand and develop various research designs
3. Collect the data by various methods: observation, interview, questionnaires
4. Analyse problem by statistical techniques: ANOVA, F-test, Chi-square
5. Understand apply for patent and copyrights

UNIT - I

Research Methodology: Objectives and Motivation of Research, Types of Research, research approaches, Significance of Research, Research Methods Verses Methodology, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India, Benefits to the society in general. Defining the Research Problem: Selection of Research Problem, Necessity of Defining the Problem

UNIT - II

Literature Survey and Report writing: Importance and purpose of Literature Survey, Sources of Information, Assessment of Quality of Journals and Articles, Need of Review, Guidelines for Review, Record of Research Review.

Report writing: Meaning of interpretation, layout of research report, Types of reports, Mechanism of writing a report. **Research Proposal Preparation**: Writing a Research Proposal and Research Report, Writing Research Grant Proposal.

UNIT - III

Research Design: Meaning of Research Design, Need of Research Design, Feature of a Good Design, Important Concepts Related to Research Design, Different Research Designs, Basic Principles of Experimental Design, Developing a Research Plan, Steps in sample design, types of sample designs.

UNIT - IV

Data Collection and Analysis: Methods of data collection, Data organization, Methods of data grouping, Diagrammatic representation of data, Graphic representation of data. Importance of Parametric, non-parametric test, testing of variance of two normal populations, use of Chi-square, ANOVA, F-test, z-test

UNIT - V

Intellectual Property Rights: Meaning, Nature, Classification and protection of Intellectual Property, The main forms of Intellectual Property, Concept of Patent, Patent document, Invention protection, Granting of patent, Rights of a patent, Licensing, Transfer of technology.

Suggested Readings:

1. C.R Kothari, Research Methodology, Methods & Technique‖; New Age International Publishers, 2004
2. R. Ganesan, Research Methodology for Engineers‖, MJP Publishers, 2011
3. Y.P. Agarwal, Statistical Methods: Concepts, Application and Computation‖, Sterling Publications Pvt. Ltd., New Delhi, 2004
4. G.B. Reddy, Intellectual Property Rights and the Law 5th Ed. 2005, Gogia Law Agency
5. Ajit Parulekar and Sarita D'Souza, Indian Patents Law – Legal & Business Implications, Macmillan India Ltd, 2006

Course Code	Course Title						Core/Elective
OE 9101 CE	**Cost Management of Engineering Projects**						**Open Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- To apply modern software packages to conduct analysis of real world data.
- To understand the technical underpinning of engineering economic analysis.
- The ability to apply the appropriate analytical techniques to a wide variety of real world problems and data sets.
- To summarize and present the analysis results in a clear and coherent manner.

Course Outcomes

At the end of this course, students will be able to**:**

1. Students should be able to learn the cost concepts in decision making
2. Student should be able to do cost planning and Marginal Costing
3. Students should be able to create a database for operational control and decision making.

UNIT-I

Introduction and Overview of the Strategic Cost Management Process: Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT-II

Project: meaning, Different types, why to manage, cost overruns centers, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non-technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process.

UNIT-III

Cost Behavior and Profit Planning Marginal Costing: Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis.

Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints.

UNIT-IV

Activity-Based Cost Management: Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT-V

Quantitative techniques for cost management: Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

Suggested Readings:

1. Cost Accounting – A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting

Course Code	Course Title						Core/Elective
OE 9102 CS	**Business Analytics**						**Open Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Understand the role of business analytics within an organization
- Analyse data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization
- To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making
- To become familiar with processes needed to develop, report, and analyse business data
- Use decision-making tools/Operations research techniques
- Mange business process using analytical and management tools
- Analyse and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.
- Student will able to understand the basic rules of research formulation and procedure for obtaining patent rights

Course Outcomes

At the end of this course, students will be able to**:**

1. Students will demonstrate knowledge of data analytics
2. Students will demonstrate the ability of think critically in making decisions based on data and deep analytics
3. Students will demonstrate the ability to use technical skills in predicative and prescriptive modelling to support business decision-making
4. Students will demonstrate the ability to translate data into clear, actionable insights

UNIT-I

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics.

Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

UNIT-II

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT-III

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

UNIT-IV

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT-V

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without 8 Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

Recent Trends in Embedded and collaborative business intelligence, Visual data 4 recovery, Data Storytelling and Data journalism.

Suggested Readings:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

Course Code	Course Title						Core/Elective
OE 9103 EC	**Embedded System Design**						**Open Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Detailed overview of important concepts of Embedded system
- Analyse PIC microcontroller, its features and programming
- Describe ARM Microcontroller architectural details and instruction set
- Understand ARM Memory management
- Learn the techniques to develop an embedded system and case studies

Course Outcomes

After completing this course, the student will be able to:

1. Understand the fundamentals of the embedded system design
2. Enumerate the instruction set of ARM Processor by studying the architecture of ARM core
3. Acquire knowledge on the serial, parallel and network communication protocols.
4. Learn the embedded system design life cycle and co-design issues.
5. List the various embedded software development tools used in the design of embedded system for various applications.

UNIT I

Introduction to Embedded Systems: Overview of Embedded System Architecture, Challenges & Trends of Embedded Systems, Hardware Architecture, Software Architecture. Application areas of Embedded Systems and Categories of Embedded Systems. Embedded System Design and Co-Design issues and Design Cycle Process

UNIT II

PIC 18: Family Overview, Architecture, Instruction Set, Addressing modes. Timers, interrupts of PIC 18, Capture/Compare and PWM modules of PIC 18

UNIT III

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT IV

ARM Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instruction Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions. Exception and interrupt handling.

ARM Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation Access Permissions, Context Switch.

UNIT V

Embedded Software Development Tools, Host and Target Machines, Linkers/Locators for Embedded Software, Getting Embedded Software into the Target System. Debugging Techniques.

Case Studies: Design of Embedded Systems using Microcontrollers – for applications in the area of communications and automotives. (GSM/GPRS, CAN, Zigbee)

Suggested Readings:

1. Raj Kamal, Embedded Systems – Architecture, Programming and Design, 2nd Edition, TMH, 2008.
2. Andrew N. Sloss, Dominic Symes, Chris Wright, ARM Systems Developer's Guides – Designing & Optimizing System Software, Elsevier, 2008.
3. Mazidi, MCKinlay and Danny Causey, PIC Microcontrollers and Embedded Systems, Pearson Education, 2007
4. David.E. Simon, An Embedded Software Primer, 1st Edition, Pearson Education, 1999
5. Jonathan W. Valvano, Embedded Microcomputer Systems, Real Time Interfacing, Thomas Learning, 1999.

Course Code	Course Title						Core/Elective
OE 9104 EE	**Waste to Energy**						**Open Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- To enable students to aware about the generation of energy from the waste.

Course Outcomes

At the end of this course, students will be able to**:**

1. Students should able to learn the Classification of waste as a fuel.
2. Students should able to learn the Manufacture of charcoal.
3. Students should able to carry out the designing of gasifiers and biomass stoves.
4. Student should able to learn the Biogas plant technology.

UNIT-I

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors. Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT-II

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT-III

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT-IV

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction

UNIT-V

Biochemical conversion: Anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Suggested Readings:

1. Non-Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book, Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

Course Code	Course Title						Core/Elective
OE 9105 ME	**Industrial Safety**						**Open Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

- Causes for industrial accidents and preventive steps to be taken.
- Fundamental concepts of Maintenance Engineering.
- About wear and corrosion along with preventive steps to be taken
- The basic concepts and importance of fault tracing.
- The steps involved in carrying out periodic and preventive maintenance of various equipments used in industry

Course Outcomes

After completing this course, the student will be equipped with:

1. concepts of engineering systems safety
2. Identify the causes for industrial accidents and suggest preventive measures.
3. Identify the basic tools and requirements of different maintenance procedures.
4. Apply different techniques to reduce and prevent Wear and corrosion in Industry.
5. Identify different types of faults present in various equipments like machine tools, IC Engines, boilers etc.
6. Apply periodic and preventive maintenance techniques as required for industrial equipments like motors, pumps and air compressors and machine tools etc.

UNIT-I

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc., Safety colour codes. Fire prevention and firefighting, equipment and methods.

UNIT-II

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT-III

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT-IV

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT-V

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance.

Suggested Readings:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, McGraw Hill Publication
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London

Course Code	Course Title						Core/Elective
AD 9001 HS	**English for Research Paper Writing**						**Audit I**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**2**	**-**	**-**	**-**	**30**	**70**	**-**

Course Objectives

- Understand that how to improve your writing skills and level of readability
- Understand the nuances of language and vocabulary in writing a Research Paper.
- Develop the content, structure and format of writing a research paper.
- Produce original research papers without plagiarism

Course Outcomes

After completing this course, the student will be able to:

1. Interpret the nuances of research paper writing.
2. Differentiate the research paper format and citation of sources.
3. To review the research papers and articles in a scientific manner.
4. Avoid plagiarism and be able to develop their writing skills in presenting theresearch work.
5. Create a research paper and acquire the knowledge of how and where to publish their original research papers.

UNIT - I

Academic Writing: Meaning & Definition of a research paper– Purpose of a research paper – Scope – Benefits, Limitations – outcomes.

UNIT - II

Research Paper Format: Title – Abstract – Introduction – Discussion – Findings, Conclusion – Style of Indentation – Font size/Font types – Indexing – Citation of sources.

UNIT - III

Research Methodology: Methods (Qualitative – Quantitative) Review of Literature. Criticizing, Paraphrasing & Plagiarism.

UNIT - IV

Process of Writing a research paper: Choosing a topic - Thesis Statement – Outline – Organizing notes - Language of Research – Word order, Paragraphs – Writing first draft –Revising/Editing - The final draft and proof reading.

UNIT - V

Research Paper Publication: Reputed Journals – National/International – ISSN No, No. of volumes, Scopus Index/UGC Journals – Free publications - Paid Journal publications – Advantages/Benefits

Presentation Skills: Developing Persuasive Presentations, Structure of Presentation, Presentation Slides, Presentation Delivery, role of the audience, what to search and cite, how to establish credibility.

Suggested Readings:

1. C. R Kothari, Gaurav, Garg, ―Research Methodology Methods and Techniques‖, 4/e, New Age International Publishers.
2. Day R, ―How to Write and Publish a Scientific Paper**",** Cambridge University Press, 2006
3. MLA Hand book for writers of Research Papers‖, 7/e, East West Press Pvt. Ltd, New Delhi
4. Lauri Rozakis, Schaum's Quick Guide to Writing Great Research Papers‖, Tata McGraw Hills Pvt. Ltd, New Delhi.

Course Code	Course Title						Core/Elective
AD 9002 CE	**Disaster Management**						**Audit I**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**2**	**-**	**-**	**-**	**30**	**70**	**-**

Course Objectives

- To impart knowledge in students about the nature, causes, consequences and mitigation measures of the various natural disasters
- To enable the students to understand risks, vulnerabilities and human errors associated with human induced disasters
- To enable the students to understand and assimilate the impacts of any disaster on the affected area depending on its position/ location, environmental conditions, demographic, etc.

Course Outcomes

At the end of this course, students will be able to**:**

1. Learn to demonstrate a critical understanding of key concepts in disaster risk reduction
2. and humanitarian response.
3. Critically evaluate disaster risk reduction and humanitarian response policy and Practice from multiple perspectives.
4. Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
5. Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in**.**

UNIT-I

Introduction: Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT-II

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem.

Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III

Disasters Prone Areas in India: Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-IV

Disaster Preparedness: Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival. Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Suggested Readings:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies", New Royal Book Company.
2. Sahni, Pardeep (Eds.), "Disaster Mitigation Experiences and Reflections", PHI, New Delhi.
3. Goel S. L., "Disaster Administration and Management Text and Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi.

Course Code	Course Title						Core/Elective
AD 9003 HS	**Sanskrit for Technical Knowledge**						**Audit I**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**2**	**-**	**-**	**-**	**30**	**70**	**-**

Course Objectives

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- To make the novice Learn the Sanskrit to develop the logic in mathematics, science & other subjects
- To explore the huge knowledge from ancient Indian literature

Course Outcomes

At the end of this course, students will be able to**:**

1. Develop passion towards Sanskrit language
2. Decipher the latent engineering principles from Sanskrit literature
3. Correlates the technological concepts with the ancient Sanskrit history.
4. Develop knowledge for the technological progress
5. Explore the avenue for research in engineering with aid of Sanskrit

UNIT-I

Introduction to Sanskrit Language: Sanskrit Alphabets-vowels-consonants- significance of Amarakosa-parts of Speech-Morphology-creation of new words-significance of synonyms-sandhi-samasa-sutras-active and passive Voice-Past/Present/Future Tense-Syntax-Simple Sentences (elementary treatment only)

UNIT-II

Role of Sanskrit in Basic Sciences: Brahmagupthas lemmas (second degree indeterminate equations), sum of squares of n-terms of AP- sulba, sutram or baudhayana theorem (origination of Pythagoras theorem)-value of pie-Madhava's sine and cosine theory (origination of Taylor's series).

The measurement system-time-mass-length-temp, Matter elasticity-optics-speed of light (origination of Michaelson and Morley theory).

UNIT-III

Role of Sanskrit in Engineering-I (Civil, Mechanical, Electrical and Electronics Engineering):

Building construction-soil testing-mortar-town planning-Machine definition-crucible-furnace-air blower-Generation of electricity in a cell-magnetism-Solar system-Sun: The source of energy, the earth-Pingala chandasutram (origination of digital logic system)

UNIT-IV

Role of Sanskrit in Engineering-II (Computer Science Engineering & Information Technology): Computer languages and the Sanskrit languages-computer command words and the vedic command words-analogy of pramana in memamsa with operators in computer language-sanskrit analogy of physical sequence and logical sequence, programming.

UNIT-V

Role of Sanskrit in Engineering-III (Bio-technology and Chemical Engineering): Classification of plants- plants, the living-plants have senses-classification of living creatures, Chemical laboratory location and layout- equipment-distillation vessel-kosthi yanthram

Suggested Readings:

1. M Krishnamachariar, History of Classical Sanskrit Literature, TTD Press, 1937.
2. M.R. Kale, A Higher Sanskrit Grammar: For the Use of School and College Students, Motilal Banarsidass Publishers, 2015.
3. Kapail Kapoor, Language, Linguistics and Literature: The Indian Perspective, ISBN- 10: 8171880649, 1994.
4. Pride of India, Samskrita Bharati Publisher, ISBN: 81-87276 27-4, 2007.
5. Shri Rama Verma, Vedas the source of ultimate science, Nag publishers, 2005.

Course Code	Course Title						Core/Elective
AD 9004 HS	**Value Education**						**Audit I**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**2**	**-**	**-**	**-**	**30**	**70**	**-**

Course Objectives

- Understand the need and importance of Values for self-development and for National development.
- Imbibe good human values and Morals
- Cultivate individual and National character.

Course Outcomes

After completion of the course, students will be able to:

1. Gain necessary Knowledge for self-development
2. Learn the importance of Human values and their application in day to day professional life.
3. Appreciate the need and importance of interpersonal skills for successful career and social life
4. Emphasize the role of personal and social responsibility of an individual for all-round growth.
5. Develop a perspective based on spiritual outlook and respect women, other religious practices, equality, non-violence and universal brotherhood.

UNIT-I

Human Values, Ethics and Morals: Concept of Values, Indian concept of humanism, human values; Values for self-development, Social values, individual attitudes; Work ethics, moral and non- moral behaviour, standards and principles based on religion, culture and tradition.

UNIT-II

Value Cultivation, and Self-management: Need and Importance of cultivation of values such as Sense-of Duty, Devotion to work, Self-reliance, Confidence, Concentration, Integrity & discipline, and Truthfulness.

UNIT-III

Spiritual outlook and social values: Personality and Behavior, Scientific attitude and Spiritual (soul) outlook; Cultivation of Social Values Such as Positive Thinking, Punctuality, Love & Kindness, avoiding fault finding in others, Reduction of anger, forgiveness, Dignity of labour, True friendship, Universal brotherhood and religious tolerance.

UNIT-IV

Values in Holy Books: Self-management and Good health; internal & external cleanliness, Holy books versus Blind faith, Character and Competence, Equality, Nonviolence, Humility, Role of Women.

UNIT-V

Dharma, Karma and Guna: Concept of soul; Science of Reincarnation, Character and Conduct, Concept of Dharma; Cause and Effect based Karma Theory; The qualities of Devine and Devilish; Satwic, Rajasic and Tamasic gunas.

Suggested Readings:

1. Chakroborty, S.K., Values & Ethics for organizations Theory and practice‖, Oxford University Press, New Delhi, 1998.
2. Jaya Dayal Goyandaka, Srimad Bhagavad Gita with Sanskrit Text, Word Meaning and Prose Meaning‖, Gita Press, Gorakhpur, 2017.

Course Code	Course Title						Core/Elective
AD 9011 HS	**Constitution of India and Fundamental Rights**						**Audit II**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**2**	**-**	**-**	**-**	**30**	**70**	**-**

Course Objectives

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective and to address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.

Course Outcomes

At the end of this course, students will be able to**:**

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

UNIT-I

History of Making of the Indian Constitution: History, Drafting Committee, (Composition & Working) Philosophy of the Indian Constitution: Preamble, Salient Features.

UNIT-II

Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT-III

Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications. Powers and Functions.

UNIT-IV

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative CEO of Municipal Corporation, Panchayat raj: Introduction, PRI: Zilla Panchayat, Elected officials and their roles, CEO Zilla Panchayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Suggested Readings:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Code	Course Title						Core/Elective
AD 9012 HS	**Pedagogy Studies**						**Audit II**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**2**	**-**	**-**	**-**	**30**	**70**	**-**

Course Objectives

- To present the basic concepts of design and policies of pedagogy studies.
- To provide understanding of the abilities and dispositions with regard to teaching techniques, curriculum design and assessment practices.
- To familiarize various theories of learning and their connection to teaching practice.
- To create awareness about the practices followed by DFID, other agencies and otherresearchers.
- To provide understanding of critical evidence gaps that guides the professional development

Course Outcomes

At the end of this course, students will be able to**:**

1. Illustrate the pedagogical practices followed by teachers in developing countries both in formal and informal classrooms.
2. Examine the effectiveness of pedagogical practices.
3. Understand the concept, characteristics and types of educational research and perspectives of research.
4. Describe the role of classroom practices, curriculum and barriers to learning.
5. Understand Research gaps and learn the future directions.

UNIT-I

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology - Theories of learning, Curriculum, Teacher education - Conceptual framework, Research questions, Overview of methodology and Searching.

UNIT-II

Thematic Overview: Pedagogical practices followed by teachers in formal and informal classrooms in developing countries - Curriculum, Teacher education

UNIT-III

Evidence on the Effectiveness of Pedagogical Practices: Methodology for the in depth stage: quality assessment of included studies - How can teacher education (curriculum and Practicum) and the school curriculum and guidance material best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches – Teachers attitudes and beliefs and pedagogic strategies.

UNIT-IV

Professional Development: alignment with classroom practices and follow up support - Support from the head teacher and the community – Curriculum and assessment - Barriers to learning: Limited resources and large class sizes.

UNIT-V

Research Gaps and Future Directions: Research design – Contexts – Pedagogy - Teacher education - Curriculum and assessment – Dissemination and research impact.

Suggested Readings:

1. Ackers J, Hardman F, Classroom Interaction in Kenyan Primary Schools, Compare‖, 31 (2): 245 – 261, 2001.
2. Agarwal M, Curricular Reform in Schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361 – 379, 2004.
3. Akyeampong K, Teacher Training in Ghana – does it count? Multisite teacher education research project (MUSTER), Country Report 1. London: DFID, 2003.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J, Improving teaching and learning of Basic Maths and Reading in Africa: Does teacher Preparation count? International Journal Educational Development, 33 (3): 272- 282, 2013.
5. Alexander R J, Culture and Pedagogy: International Comparisons in Primary Education, Oxford and Boston: Blackwell, 2001.
6. Chavan M, Read India: A mass scale, rapid, learning to read campaign, 2003.

Course Code	Course Title						Core/Elective
AD 9013 HS	**Stress Management by Yoga**						**Audit II**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**2**	**-**	**-**	**-**	**30**	**70**	**-**

Course Objectives

The Course will introduce the students to

- Creating awareness about different types of stress and the role of yoga in the management of stress.
- Promotion of positive health and overall wellbeing (Physical, mental, emotional, social and spiritual).
- Prevention of stress related health problems by yoga practice.

Course Outcomes

After successful completion of the course, the students will be able to:

1. Understand yoga and its benefits.
2. Enhance Physical strength and flexibility.
3. Learn to relax and focus.
4. Relieve physical and mental tension through asanas.
5. Improve work performance and efficiency.

UNIT - I

Meaning and Definition of Yoga - Historical perspective of Yoga - Principles of Astanga Yoga by Patanjali.

UNIT - II

Meaning and Definition of Stress - Types of stress - Eustress and Distress. Anticipatory Anxiety and Intense Anxiety and depression. Meaning of Management- Stress Management.

UNIT - III

Concept of Stress According to Yoga - Stress assessment methods - Role of Asana, Pranayama and Meditation in the management of stress

UNIT - IV

Asanas- (5 Asanas in each posture) - Warm up - Standing Asanas - Sitting Asanas - Prone Asanas - Supine asanas - Surya Namaskar.

UNIT - V

Pranayama- Anulom and Vilom Pranayama - Nadishudhi Pranayama - Kapalabhati Pranayama - Bhramari Pranayama - Nadanusandhana Pranayama.

Meditation Techniques: Om Meditation - Cyclic meditation: Instant Relaxation technique (QRT), Quick Relaxation Technique (QRT), Deep Relaxation Technique (DRT)

Suggested Readings:

1. "Yogic Asanas for Group Training - Part-I", Janardhan Swami Yogabhyasi Mandal, Nagpur.
2. Swami Vivekananda, "Rajayoga or Conquering the Internal Nature", Advaita Ashrama (Publication Department), Kolkata.
3. Nagendra H.R and Nagaratna R, "Yoga Perspective in Stress Management", Swami Vivekananda Yoga Prakashan, Bangalore.

Course Code	Course Title						Core/Elective
AD 9014 HS	**Personality Development Through Life Enlightenment Skills**						**Audit II**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**2**	**-**	**-**	**-**	**30**	**70**	**-**

Course Objectives

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes

At the end of this course, students will be able to**:**

1. Develop their personality and achieve their highest goal of life.
2. Lead the nation and mankind to peace and prosperity.
3. Practice emotional self-regulation.
4. Develop a positive approach to work and duties.
5. Develop a versatile personality.

UNIT - I

Neetisatakam – Holistic Development of Personality - Verses 19, 20, 21, 22 (Wisdom) - Verses 29, 31, 32 (Pride and Heroism) - Verses 26,28,63,65 (Virtue)

UNIT - II

Neetisatakam – Holistic Development of Personality (cont'd) - Verses 52, 53, 59 (don'ts) – Verses 71,73,75 & 78 (do's) - Approach to day to day works and duties.

UNIT - III

Introduction to Bhagavadgeetha for Personality Development - Shrimad Bhagavadgeetha: Chapter 2 – Verses 41, 47, 48 - Chapter 3 – Verses 13,21,27,35 - Chapter 6 – Verses 5,13,17,23,35 - Chapter 18 –Verses 45, 46, 48 Chapter – 6: Verses 5, 13, 17, 23, 35; Chapter – 18: Verses 45, 46, 48

UNIT - IV

Statements of Basic Knowledge - Shrimad Bhagavadgeetha: Chapter 2- Verses 56, 62,68 - Chapter 12 – Verses 13, 14, 15, 16, 17, 18 - Personality of Role model from Shrimad Bhagawat Geeta.

UNIT - V

Role of Bhagavadgeetha in the Present Scenario - Chapter 2 – Verses 17 - Chapter 3 – Verses 36, 37, 42 - Chapter 4 – Verses 18, 38, 39 - Chapter 18 – Verses 37, 38, 63.

Suggested Readings:

1. Srimad Bhagavad Gita, Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya), P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi

Online Resources: NTPEL: http://nptel.ac.in/downloads/109104115/

Course Code	Course Title						Core/Elective
PC 3351 EV	**Embedded Systems Lab**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**-**	**-**	**-**	**2**	**50**	**-**	**1**

Course Outcomes

After completing this course, the student will be able to:

1. Use the IDE tool effectively for developing and executing the programs using 8051.
2. Comprehend the usage of on-chip timers and serial communication of 8051 and their interrupts using programs
3. Interface devices like ADC, DAC, LCD, and Stepper Motor to 8051 and develop real time projects.
4. Use the Kiel software for the development of logic, Proteus software for hardware simulation and flash magic for downloading the code on to the target system.
5. Develop the logic to interface devices like temp sensor, stepper motor, Buzzer to ARM microcontroller and analyse the working of GPIO, on-chip peripherals of ARM

Cycle 1: Programming in 8051

1. Study of 8051 Evaluation Board Trainer kit and Keil IDE Software Tool.
2. Serial Data Transmission
3. Interface switches and LEDs
4. Interface LCD
5. Interface 4*4 matrix keyboard
6. Interface stepper motor
7. Interface 7 Segment Display using I2C
8. ADC, DAC Interface

Cycle 2: Programming in LPC2148 ARM Processor

1. Configure and Control General Purpose I/O Pins
2. Interfacing LED & Switch Interface
3. 2*16 LCD Display
4. Serial Communication
5. I2C Interface & EEPROM Interface
6. Buzzer Interface
7. SD-MMC Card Interface

Note: all the experiments are to be carried out independently by each student with different specifications. At least 12 experiments are to be carried out.

Course Code	Course Title						Core/Elective
PC 3352 EV	**Real Time Operating Systems Lab**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**-**	**-**	**-**	**2**	**50**	**-**	**1**

Course Outcomes

After completing this course, the student will be able to:

1. Understand the concept of file system calls and process system calls by programming in UNIX operating system
2. Comprehend the concepts of RTOS and demonstrate them in ARM microcontroller
3. Simulate the timing concepts, scheduling algorithms and semaphores using VxWorks

List of Experiments:

1. Write an embedded C program to demonstrate on ARM Micro controller Kit
    a. Round Robin Task Scheduling
    b. Preemptive Priority Based Task Scheduling
    c. Priority Inversion
    d. Timing Concept
    e. Message and Queues
    f. Semaphores
    g. Multi Tasking concept of Real Time Application
2. Write the pseudo code in Linux using C/C++ to perform Print parent process ID & child process ID using Fork()
3. Study of POSIX thread & Write appropriate the pseudo code in Linux using C/C++
4. Study of Dining Table philosophy problem and write appropriate pseudo code for the same

Course Code	Course Title						Core/Elective
PC 3353 EV	**VLSI Lab**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**-**	**-**	**-**	**2**	**50**	**-**	**1**

Course Outcomes

After completing this course, the student will be able to:

1. Draw the designs using schematic editor and simulate them using Mentor Graphics EDA tool
2. Simulate and analyse DC, AC and Transient response of Amplifier circuits using different types of current mirrors.
3. Draw layouts of logic gates (NOT,NAND,NOR) and perform DRC ,LVS and RC extractions.

List of Experiments:

1. Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
    a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS determine Vt
    b. Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
    c. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
    d. Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV

    To extract Vth use the following procedure.

    i. Plot gm vs VGS using NGSPICE and obtain peak gm point.
    ii. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice.
    iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
    iv. Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.

    Tabulate your result according to technologies and comment on it.
2. Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.

    Perform the following

    a. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
    b. Plot VTC for CMOS inverter with varying VDD.
    c. Plot VTC for CMOS inverter with varying device ratio.
    d. Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF)
    e. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k)
3. Use CAD tools to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

    Perform the following

    a. Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at

the switching point using CAD tools and compare the values for 0.18um and 0.13um process.

b. Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.

c. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.

4. Calculate input bias voltage if bias current=50uA.
   a. Use CAD Tools and obtain the bias current. Compare its value with 50uA.
   b. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in CAD Tools (consider 30fF load capacitance).
   c. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW
5. Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA.
   Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
   a. Draw the schematic of op-amp macro model.
   b. Draw the schematic of INA.
   c. Obtain parameters of the op-amp macro model such that
      i. low-frequency voltage gain = 5x104,
      ii. unity gain BW (fu) = 500KHz,
      iii. input capacitance=0.2pF,
      iv. output resistance = ,
      v. CMRR=120dB

Course Code	Course Title						Core/Elective
PC 3354 EV	**Seminar**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	-	-	-	**2**	**50**	-	**1**

Course Outcomes

At the end of this course, students will be able to**:**

1. Develop the habit of referring the journals for literature review.
2. Understand the gist of the research paper.
3. Identify the potential for further scope.
4. Present the work in an efficient manner.
5. Write the documentation in standard format.

Seminar topics may be chosen by the students with advice from the faculty members and the student shall read further relevant articles in the domain.

The seminar must be clearly structured and the power point presentation shall include following aspects:

1. Introduction to the field
2. Literature survey
3. Consolidation of available information
4. Summary and Conclusions
5. References

Each student is required to:

1. Deliver the seminar for a maximum duration of 30 minutes, where the presentation should be for 20 minutes in PowerPoint, followed by Question and Answers session for 10 minutes.
2. Submit the detailed report of the seminar in spiral bound in a précised format as suggested by the Department.

Guidelines for awarding marks		
S. No.	**Description**	**Max. Marks**
1	Contents and relevance	10
2	Presentation skills	10
3	Preparation of PPT slides	05
4	Questions and answers	05
5	Report in a prescribed format	20

Note:

1. The seminar presentation should be a gist of at least five research papers from **Peer-reviewed** or **UGC recognised** journals.
2. **The seminar report should be in the following order:** Background of work, literature review, techniques used, prospective deliverables, discussion on results, conclusions, critical appraisal and reference.
3. At least two faculty members will be associated with the seminar presentation to evaluate and award marks.
4. Attendance of all the students for weekly seminar presentations is compulsory. If the student fails to secure minimum attendance as per O.U. rules, the marks awarded in the seminar presentation shall remain void.

Course Code	Course Title						Core/Elective
PC 3355 EV	**Mini Project with Seminar**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**-**	**-**	**-**	**4**	**50**	**-**	**2**

Course Outcomes

At the end of this course, students will be able to**:**

1. Formulate a specific problem and give solution
2. Develop model/models either theoretical/practical/numerical form
3. Solve, interpret/correlate the results and discussions
4. Conclude the results obtained
5. Write the documentation in standard format

Guidelines:

- As part of the curriculum in the II- semester of the programme each student shall do a mini project, generally comprising about three to four weeks of prior reading, twelve weeks of active research, and finally a presentation of their work for assessment.
- Each student will be allotted to a faculty supervisor for mentoring.
- Mini projects should present students with an accessible challenge on which to demonstrate competence in research techniques, plus the opportunity to contribute something more original.
- Mini projects shall have inter-disciplinary/ industry relevance.
- The students can select a mathematical modeling based/Experimental investigations or Numerical modeling
- All the investigations should be clearly stated and documented with the reasons/explanations.
- The mini-project shall contain a clear statement of the research objectives, background of work, literature review, techniques used, prospective deliverables, and detailed discussion on results, conclusions and reference

Departmental committee: Supervisor and a minimum of two faculty members

Guidelines for awarding marks in CIE (Continuous Internal Evaluation): Max. Marks: 50		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	20	Progress and Review
	05	Report
Departmental Committee	05	Relevance of the Topic
	05	PPT Preparation
	05	Presentation
	05	Question and Answers
	05	Report Preparation

Course Code	Course Title						Core/Elective
PC 3356 EV	**Major Project Phase – I**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	-	-	-	**20**	**100**	-	**10**

Course Outcomes

At the end of this course, students will be able to:

1. Exposed to self-learning various topics.
2. Learn to survey the literature such asbooks, journals and contact resource persons for the selected topic of research.
3. Learn to write technical reports.
4. Develop oral and written communication skills to present.
5. Defend their work in front of technically qualified audience

Guidelines:

- The Project work will preferably be a problem with research potential and should involve scientific research, design, generation/collection and analysis of data, determining solution and must preferably bring out the individual contribution.
- Seminar should be based on the area in which the candidate has undertaken the dissertation work.
- The CIE shall include reviews and the preparation of report consisting of a detailed problem statement and a literature review.
- The preliminary results (if available) of the problem may also be discussed in the report.
- The work has to be presented in front of the committee consists of Chairperson-BoS, Osmania University and Head, Supervisor & Project coordinator from the respective Department of the Institute.
- The candidate has to be in regular contact with his supervisor and the topic of dissertation must be mutually decided by the guide and student.

Guidelines for awarding marks in CIE (Continuous Internal Evaluation): Max. Marks: 100		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	30	Project Status / Review(s)
	20	Report
Departmental Committee (Chairperson BoS, Osmania University and Head, Supervisor & Project coordinator from the respective department of the institution)	10	Relevance of the Topic
	10	PPT Preparation
	10	Presentation
	10	Question and Answers
	10	Report Preparation

Note: The Supervisor has to assess the progress of the student regularly.

Course Code	Course Title						Core/Elective
PC 3357 EV	**Major Project Phase – II (Dissertation)**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	-	-	-	**32**	-	**200**	**16**

Course Outcomes

At the end of this course, students will be able to:

1. Use different experimental techniques and will be able to use different software/ computational /analytical tools.
2. Design and develop an experimental set up/ equipment/test rig.
3. Conduct tests on existing set ups/equipments and draw logical conclusions from the results after analysing them.
4. Either work in a research environment or in an industrial environment.
5. Conversant with technical report writing and will be able to present and convince their topic of study to the engineering community.

Guidelines:

- It is a continuation of Major Project Phase – I started in semester - III.
- The student has to submit the report in prescribed format and also present a seminar.
- The dissertation should be presented in standard format as provided by the department.
- The candidate has to prepare a detailed project report consisting of introduction of the problem, problem statement, literature review, objectives of the work, methodology (experimental set up or numerical details as the case may be) of solution and results and discussion.
- The report must bring out the conclusions of the work and future scope for the study. The work has to be presented in front of the examiners panel consisting of an approved external examiner and Chairperson BoS, & Head, Osmania University and Supervisor from the Institute.
- The candidate has to be in regular contact with his/her Supervisor / Co- Supervisor

Guidelines for awarding marks in SEE (Semester End Examination): Max. Marks: 200		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	10	Regularity and Punctuality
	10	Work Progress
	30	Quality of the work which may lead to publications
	10	Analytical / Programming / Experimental Skills Preparation
	10	Report preparation in a standard format
External Examiner and Chairperson, BoS & Head, Osmania University (All together)	20	Power Point Presentation
	60	Quality of thesis and evaluation
	30	Innovations, application to society and Scope for future study
	20	Viva-Voce